LISTING OF THE CLAIMS

1. (original) A high density read-only memory (ROM) cell installed on a silicon substrate for storing data, comprising:

a first doped region being of a second conductive type installed on the silicon substrate;

a plurality of first heavily doped regions being of a first conductive type installed in the first doped region;

a second doped region being of the second conductive type installed on the silicon substrate; and

a gate installed on the surface of the silicon substrate and adjacent to the first doped region and the second doped region.

2. (original) The ROM cell of claim 1 installed in a doped well being of the first conductive type on the silicon substrate.

3. (original) The ROM cell of claim 1 wherein the first conductive type is P-type, and the second conductive type is N-type.

4. (original) The ROM cell of claim 1 wherein the first conductive type is N-type, and the second conductive type is P-type.

5. (original) The ROM cell of claim 1 wherein the first doped region is a drain doped region and the second doped region is a source doped region, and each of the plurality of heavily doped regions and the first doped region form a diode so that a plurality of drain signals respectively passing through the plurality of heavily doped regions do not interfere with each

other.

6. (previously presented) A high density ROM cell installed on a silicon substrate for storing data, comprising:

a plurality of drain doped regions being of a second conductive type installed on the silicon substrate;

a source doped region being of the second conductive type installed on the silicon substrate; and

a gate installed on the surface of the silicon substrate and adjacent to the plurality of drain doped regions and the source doped region, the gate having at least one extension structure respectively located between one of the plurality of drain doped regions and another drain doped region so that a plurality of drain signals respectively passing through the plurality of drain doped regions do not interfere with each other.

7. (previously presented) The ROM cell of claim 6 installed in a doped well being of a first conductive type on the silicon substrate.

8. (original) The ROM cell of claim 7 wherein the first conductive type is P-type, and the second conductive type is N-type.

9. (original) The ROM cell of claim 7 wherein the first conductive type is N-type, and the second conductive type is P-type.

10. (original) The ROM cell of claim 6 wherein the second conductive type is N-type.

11. (original) The ROM cell of claim 6 wherein the second conductive type is P-type.

12. (cancelled)